SEMICONDUCTOR DEVICE POWER DISTRIBUTION SYSTEM AND METHOD

[0001] The present application is a divisional of Application Serial No. 10/051965 filed January 16, 2002, the contents of which is incorporated herein by reference.

TECHNICAL FIELD

[0002] This invention relates to power and signal distribution in semiconductor dies.

BACKGROUND

[0003] Many conventional semiconductors are mounted in packages such as Quad Flat Packs (QFPs) and Pin Ball Gate Arrays (PBGAs) in which the input and output terminals are arranged along the edge of the die. Arranging the terminals along the die edge may result in relatively long wirings on silicon to supply power and ground to the center of the die. These long wirings generally have a relatively high resistance leading to unacceptable IR voltage drops.

SUMMARY OF THE INVENTION

[0004] An integrated circuit power distribution system and method is provided. The integrated circuit comprises a

semiconductor die that includes at least one pair of bond pads having a single bond wire connected thereto such that each bond pad of the pair of bond pads has only one bond wire end connected thereto. A first bond pad of the pair of bond pads is located in an internal portion of the semiconductor die. A first wire having a first end and a second end is electrically connected between the pair of bond pads.

DESCRIPTION OF DRAWINGS

[0005] FIG. 1 is a two-dimensional top-view of a semiconductor device.

[0006] FIG. 2 is a two-dimensional side-view of a semiconductor device.

[0007] FIG. 3 is a two-dimensional side-view of a semiconductor device.

[0008] FIG. 4 is a two-dimensional side-view of a semiconductor device.

[0009] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0010] Figure 1 shows a top-view of a semiconductor power distribution system and method. A semiconductor device 10 includes a semiconductor die 12 and several lead fingers 14a-14h. The semiconductor device 10 may be mounted in any suitable package such as QFPs and PBGAs.

[0011] The semiconductor die 12 includes bonding surfaces 16 arranged in an interior portion 18 of the semiconductor die 12 as well as along an outer periphery 20 of the semiconductor die 12. The bonding surfaces 16 are preferably bonding pads connected to traces in the semiconductor die 12. The bonding surfaces 16 provide connection points for lead wires 22 extending to other bonding surfaces 16 or lead fingers 14. Employing a lead wire 22 within the interior portion 18 may advantageously reduce the voltage drop caused by IR losses in a trace. In addition, a lead wire 22 may be used in place of a trace to reduce the density of traces within the semiconductor die 12. Using a lead wire 22 to couple electrical signals to internal portions of the semiconductor 12 may be particularly advantageous in high density semiconductors where using wide low resistance traces to carry the signal would require additional layers. In one example, a lead wire 22 may be connected in parallel with a trace in the semiconductor die 18 to reduce the combined resistance, thereby decreasing the voltage drop

associated with the trace. In a second example, a lead wire 22 may be used in lieu of using a trace within the semiconductor die 18. In a third example, a lead wire may be connected from a bonding surface 16 located along one edge of the semiconductor periphery 20 to another bonding surface 16 located along another edge of the semiconductor periphery 20.

[0012] The lead wires 22 are bonded to different ones of the bonding surfaces 16 and/or lead finger 14 to provide low resistance connections for electrical signals such as power, ground, and signals. The lead wires 14 may comprise an electrically conductive material such as gold, aluminum, and copper that has a low electrical resistance. Each of the lead fingers 14 may be coupled to a bonding surface or remain as a non-connected lead finger 14h. Any wire bonding method such as thermocompression and ultrasonic may be used to bond the lead wires 14 to the bonding surfaces 16 and lead fingers 14.

[0013] The lead wires 22 may be bonded using any wire bond type such as ball bond, stitch bond on bonding pad, and stitch bond on ball. A ball bond may be formed by first forming a sphere at the end of a lead wire. Then, the sphere is pressed against a bonding surface for a few seconds to form a weld. A stitch bond on bonding pad may be formed by placing the tail of a lead parallel to a bonding surface. Then, pressure is applied to the lead wire forcing the lead wire onto the bonding pad. A stitch

bond on ball may be formed in similar manner to forming a stitch bond on bonding pad, except a ball is first formed on the bonding surface.

[0014] Figure 2 shows another aspect of the semiconductor power distribution system. A lead wire 30 is connected in parallel with a trace 32 to reduce the electrical resistance of a connection between two bonding surfaces 34a and 34b. The lead wire 30 may be connected via a trace 36 to another lead wire 38 that is connected to a lead finger 40. The lead wire 30 reduces the voltage losses associated with the electrical resistance of the trace 32 by providing a parallel path for current.

[0015] Figure 3 shows another aspect of the semiconductor power distribution system and method. A lead wire 50 is connected between two bonding surfaces 52a and 52b. The bonding surface 52b is preferably located within an interior portion 62 of a semiconductor die 64. The lead wire 50 is used in lieu of a trace to carry electrical signals between the bonding surfaces 52a and 52b. The lead wire 50 may be coupled to the bonding surfaces 52a and 52b via a ball bond 54 and a stitch bond on ball 56 respectively. Another lead wire 58 may connect the bonding surface 52a to a lead finger 60 so that signals may be coupled between the lead finger 60 and the interior portion 62 of the semiconductor die 64 without traversing within the semiconductor die 64.

[0016] Figure 4 shows another aspect of the semiconductor power distribution system and method similar to that shown in Figure 2 in function with corresponding elements numbered in the range 70 to 80, except that the lead wire 70 is connected at bonding surface 74b with a stitch on pad type of bond.

[0017] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.